PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jianhua Sun et al.
Application No.	:	10/795,796
Filed	:	March 8, 2004
For	:	METHOD FOR PROCESSING A DIGITAL VIDEO AUDIO SIGNAL

Examiner	:	Asher R. Khan
Art Unit	:	4134
Docket No.	:	851663.465
Date	:	July 14, 2008

DECLARATION OF RICHARD W. KORALEK, Ph.D.
PURSUANT TO 37 C.F.R. §1.132

I, Richard W. Koralek, Ph.D. declare as follows:

1. I have been retained by STMicroelectronics, Inc., to analyze some of the prior art cited with respect to the above-identified patent application to Sun *et al.* (hereinafter "the Sun application").

2. I hold a Bachelor of Science degree (1966) in Electrical Engineering from the Massachusetts Institute of Technology, and a Master of Science degree (1967) and Doctor of Philosophy degree (1972) in Electrical Engineering from Stanford University.

3. I have more than thirty years experience as an academic, industry practitioner, and expert witness. My expertise includes management, design, and development in telecommunications, signal processing systems, modem development, and integrated circuit development. My technology expertise encompasses error-correcting codes, telecommunications, digital signal processing (both algorithms and implementation), digital systems design, communications theory, integrated circuit design, and CAD.

4. I have received various patents and awards for my efforts in the fields of communications and VLSI circuits.

5. I provide support for technical patent prosecution, licensing, and litigation in the areas of communications, modems, digital signal processing (DSP), digital video and audio, and error-correcting codes.

6. I have been an expert witness on several occasions, and have been deposed and testified at arbitrations, bench and jury trials, and at Markman hearings. A copy of my curriculum vitae is attached hereto as Exhibit 1.

7. I am familiar with the Sun application. I have reviewed Applicants' Amendment, filed July 14, 2008, and the outstanding final Office Action mailed on November 25, 2008. I have also reviewed the following references cited in the outstanding final Office Action: US Patent 6,226,443 to Morioka et al ("Morioka"), KR Patent Application 10-1996-0072736 to Kim ("Kim"), and US Patent 6,876,814 to Le Dantec ("Le Dantec"). The outstanding Office Action relies on Applicants' Admitted Prior Art (AAPA), the section of the Sun application entitled "Background of the Invention," in formulating obviousness rejections.

8. I submit this Declaration as evidence of the non-obviousness of the presently claimed methods of decoding audio data over the references cited in the aforementioned Office Action.

9. AAPA discloses that prior art methods of decoding audio data fetch an entire DIF block and then deshuffle the bytes, using a pre-computed lookup table of reverse mapping or analyzing an entire DV audio frame. The AAPA states "If the shuffled coded data may be represented as $(t_1, t_2, s_1, b_1)=f(n)$, then the reverse mapping f^{-1} may be considered to provide the correct order of data. This concept is shown in FIG. 4. However, this concept is not generally possible in practice, as the shuffling process involves modular and non-linear operations, such as $\lfloor x \rfloor$, which result in a one-to-many reverse relationship. It is therefore not generally possible to easily find a suitable reverse mapping f^{-1}." A person of ordinary skill in the art, after reading that, would understand that the use of an inverse function may not be possible for all sets of parameters, that an

inverse function may give ambiguous values of the index n, and that this would not be a fruitful direction.

10. In my opinion, Morioka teaches fetching an entire DIF frame at a time (in contrast to the claimed methods of the Sun application). Morioka describes a system, which he identifies as "a memory process" (column 18, line 45) which stores audio and video data on a hard disk. This is verified by the paragraph that states "As described above, in the memory process during the recording operation, (1) recording a DIF signal onto the DIF recording HDD 1906 and (2) converting an audio signal into a PCM signal in real time and then recording the signal onto the audio recording HDD 1907 are performed with respect the 1.times. input and the 4.times. input. " (column 19 lines 13-18) He then states "Simultaneously, in performing the recording operation 1905, only the audio blocks are extracted from the DIF; deshuffled; converted into temporally continuous PCM audio ...; and then recorded onto an audio recording HDD 1907 (or 1009)." (column 18 line 65 – column 19 line4) This suggests that an entire DIF frame is fetched and the audio blocks (plural) are extracted for deshuffling. This understanding is further supported by the immediately following discussion: "It is noted that the present inventors obtained an experimental result that, in the case of using a Pentium (clock: 100 MHz) as a CPU, the conversion time was about 0.6 msec which is sufficiently shorter than one frame period or 33.3 msec of an NTSC system. Even in the case of the 4x input, it takes 2.4 msec to perform this conversion, so that real time performance can be sufficiently secured even by the use of software processing." (column 19, lines 4-12) This discussion of real-time performance is based on the time to process an entire DIF frame versus the temporal amount of audio in a DIF frame.

11. Based on the above discussion, Morioka teaches fetching an entire DIF frame, extracting the plurality of audio blocks and then deshuffling the data for subsequent storage on the audio HDD. Thus Morioka teaches away from fetching and processing the audio data one block at a time. Furthermore, Morioka provides no detail whatsoever regarding how to perform the deshuffling operation. One of ordinary skill in the art would not be led by Morioka to look for an inverse shuffling function, but rather would look elsewhere to find a deshuffling method.

12. Kim appears to disclose a hardware structure for deshuffling that implements a prior art method described AAPA. In this method, the shuffling function, specified in Kim lines 15-24, is implemented using a set of modulo counters, and the results are either stored as an inverse mapping or used to deshuffle an entire stored DIF frame. There is no teaching of an explicit inverse function, and given that the forward function is explicitly described (equations 1-3) but no explicit inverse function is presented, a person of ordinary skill would conclude that an inverse function is not practical. Also, there is no suggestion in Kim to fetch only a single DIF block at a time (in fact, the method of Kim teaches away from this).

13. In contrast to AAPA, Morioka and Kim, the Sun application discloses deshuffling audio data contained in a Digital Video (DV) data stream, operating on a single DIF block at a time and using a deshuffling equation to reorder the audio data samples into their original sequence. The Sun application teaches fetching only a single DIF block at a time and deshuffling bytes in the block one at a time using the deshuffling equations to determine the index (location) of the byte in the original sequence.

14. In my opinion, given that the shuffling function described in AAPA is non-linear and that an inverse of the shuffling function may give ambiguous values, I am surprised by deshuffling disclosed and claimed in the Sun application.

15. In conclusion, I submit that a person of ordinary skill in the art, after reading the AAPA, would understand that the use of an inverse function may not be possible for all sets of parameters, that an inverse function may give ambiguous values of the index n, and that person of ordinary skill in the art would be discouraged from attempting to decode audio data using an inverse function. Furthermore, AAPA, Morioka and Kim, individually and collectively, fail to disclose, teach, or suggest Applicants claimed methods of decoding audio data. In particular, the cited prior art, individually and collectively, fail to disclose, teach, or suggest audio data that is encoded into multiple DIF blocks of a DV frame may be decoded one DIF block at a time by de-shuffling the bytes of a respective DIF block of the multiple DIF blocks for each respective one of the multiple DIF blocks of the DV frame.

I hereby declare that all statements made herein are, to my own knowledge, true and that all statements made on information or belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the captioned patent application or any patent issued therefrom.

Date 2/25/2009

Richard W. Koralek, Ph.D.

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Richard W. Koralek, Ph.D.
Curriculum Vitae

Professional Summary

Dr. Koralek has more than 30 years of experience as an academic, industry practitioner and litigation support and expert witness. His expertise includes management, design, and development in telecommunications, signal processing systems, modem development and integrated circuit development. Dr. Koralek's technology focus encompasses error-correcting codes, telecommunications, digital signal processing (both algorithms and implementation), digital systems design, communications theory, integrated circuit design, and CAD. Dr. Koralek is the recipient of patents and awards for his efforts in the fields of communications and VLSI circuits.

Dr. Koralek also provides support for technical patent prosecution, licensing, and litigation in the areas of communications, modems, digital signal processing (DSP), digital video and audio, and error correcting codes. He has been an expert witness on several occasions, and has been deposed and has testified at arbitration, bench trial, and at Markman hearings.

Expertise

- Adaptive Equalization
- Analog to Digital Conversion
- Communications Theory
- Digital Signal Processing
- Digital System Design
- Error Correcting Codes
- Integrated Circuit Design
- Modem Theory
- Data Compression
- Patent prosecution and litigation support

Education

Year	College or University	Degree
1972	Stanford University	Ph.D., E.E.,
1967	Stanford University	M.S.E.E.. Placed first in EE Ph.D. Qualifying Exam at Stanford, 1968
1966	Massachusetts Institute of Technology	B.S.E.E.

Professional Experience

From: 1985
To: Present
Organization: RWK Consulting Associates, Inc.
Title: President
Summary: Technical consulting with a number of major corporations and small companies in the areas of error-correcting codes, digital signal processing, modem design, IC design for DSP chips, and tape and disk drive electronics. Some specific projects include:

- Member of outside technical patent review panel for major semiconductor company, including patent review and licensing
- 2 BCH error-correcting decoders operating at up to 2 gigabits per second (for which a patent has been awarded)
- Programmable BCH/Reed-Solomon decoding chip (3 patents)
- 2400 BPS adaptively equalized modem on a chip
- Several Reed-Solomon error-correcting systems for disk drives (3 patents)
- Turbo code algorithm using block codes for ASIC implementation
- A Sigma-Delta analog-to-digital converter, several satellite communications link designs including transmitter and receiver implementations
- Unique combined modulation-coding system,
- A non-linear adaptive equalizer for QAM signals (2 patents)
- Universal modem DSP chip
- Numerous error-correcting code studies encompassing code selection, performance tradeoffs, and implementation
- PC-based video compression and transmission system
- Low end local area network for PCs
- Number of modeling and simulation studies of local area networks and backbone networks.

From: 1983
To: 1985
Organization: Cermetek Microelectronics, Inc.
Title: Vice President, Research & Development
Summary: Responsibilities encompassed management of the company's research and development and engineering activities, defining the technical direction of the company, contributing to new product and market definition, and OEM customer support and marketing. Achievements include:

- Fixing a number of major design problems with old products
- Development of 2 custom integrated circuits to implement an entire 1200bps modem (with 100% working prototypes 6 months from project initiation)
- Development of a 2400bps adaptively equalized modem
- Initiation of a 9600bps full-duplex modem using echo cancellation techniques
- Completion of a number of modem-based products.
- Active member of the CCITT Modem Working Party (Study Group XVII) and the CCITT ISDN Joint Working Group (Study Group XVIII), as well as participating in T1D1 ISDN Meetings. Built and managed an outstanding team of over 20 engineers and support people in Sunnyvale and started a 13-person product design

center in Taipei, Taiwan. Managed an R&D budget of over $1 million

From: 1982
To: 1983
Organization: Ford Microelectronics, Inc.
Title: Ford Aerospace Applications Development Manager
Summary: On the founding team of Ford Microelectronics, a wholly owned subsidiary of Ford Aerospace. The purpose of FMI was to service the custom integrated circuit needs of Ford Motor Company and Ford Aerospace by providing custom IC design services and having devices fabricated by outside foundries. Responsibilities included liaison to all divisions of Ford Aerospace, custom IC consulting for designers, training and education, and project tracking. This position afforded an excellent opportunity to develop technical marketing skills.

From: 1976
To: 1982
Organization: Ford Aerospace & Communications Corporation
Title: Senior Staff Engineer
Summary: Started with Ford on a part-time basis while on the faculty of San Jose State University. In 1979 became a full-time contributor at Ford. Managed an internal R&D program of $2 million per year for the activity. Designed a family of Viterbi-algorithm error correcting decoders, including pioneering work in VLSI decoder implementations. These included a constraint-length 5-coder/decoder chip with over 33,000 transistors implemented in a 2 micron CMOS/SOS technology. Developed a unique decoder synchronization scheme and a new decoder testing technique for VLSI. These activities resulted in 4 papers to major conferences, 2 of which won awards. A principal technical contributor on VLSI and CAD systems, including an extensive corporate study of IC CAD systems. A principal contributor to the design of several signal processing VLSI chips, one of which had nearly 50,000 transistors of random logic and operated at over 70 mega-multiplies per second. Has been a key contributor to and designer of numerous digital signal processing systems, including the design of modulator and demodulator systems, adaptive equalizers, image processing systems, spread-spectrum communications systems, and signal recognition systems using pattern recognition techniques.

From: 1974
To: 1979
Organization: San Jose State University
Title: Associate Professor, Electrical Engineering
Summary: Taught graduate and undergraduate courses in electrical engineering, communication theory, and computer science (hardware and software).

- Awarded Outstanding Professor Award by Tau Beta Pi.
- Worked at Ford Aerospace during the period 1976 - 1979.

From:	1971
To:	1974
Organization:	ESL, Inc.
Title:	Senior Member, Technical Staff
Summary:	Responsible for hardware and systems design for modems (with adaptive equalizers), satellite communication links, and signal processing systems. Some specific designs included a digital modulator and adaptive equalizer for a 4800/7200 BPS modem, several FM and FM/FM demodulators, a QAM modulator and demodulator system, and a satellite communication system. During this time, taught graduate courses at the University of Santa Clara.

Selected Litigation Support Experience

Dr. Koralek has for several years served as a technical consultant regarding intellectual property matters for a major semiconductor manufacturing company.

Expert Engagement:

Type of Matter:	Patent Infringement
Law Firm:	Orrick, Herrington & Sutcliffe LLP, Terrence P. McMahon, Esq.
Case Name:	Creative Labs v. Aureal Incorporated
Date:	1998-99
Services Provided:	Submitted Expert Reports, Testified at Deposition, Markman Hearing and Jury Trial.
Disposition:	Concluded

Expert Engagement:

Type of Matter:	Contract Dispute on Aeronautics Devices
Law Firm:	Cooley Godward LLP, Joseph P. Russoniello, Esq.
Case Name:	BEI v. Systron Donner
Date:	1993-95
Services Provided:	Testified at Arbitration on behalf of Systron Donner
Disposition:	Concluded

Expert Engagement:

Type of Matter:	Contract Dispute and Patent Infringement
Law Firm:	Brown & Bain, Martin L Lagod, Esq.
Case Name:	Exar Corporation v. GVC
Date:	1994
Services Provided:	Wrote Declaration for Exar
Disposition:	Case settled

Expert Engagement:

Type of Matter:	Patent Infringement
Law Firm:	Hopgood, Calimafde, Kalil & Judlowe LLP, Alan Pollock, Esq,
Case Name:	Crystal Semiconductor v. Analog Devices Corporation
Date:	1993-94
Services Provided:	Wrote Preliminary Report for Analog Devices
Disposition:	Case settled

Professional Affiliations, Achievements & Awards

- Member, IEEE
- Former Reviewer, IEEE Transactions on Communications.
- Past Chairman, IEEE Aerospace & Electronics Systems Society

Patents & Publications

Patent	Date	Description
7,089,276	2006	Modular Galois-Field Subfield-Power Integrated Inverter-Multiplier Circuit for Galois-Field Division Over GF(256)
6,725,411	2004	Iterated Soft-Decision Decoding of Block Codes
6,499,128	2002	Iterated Soft-Decision Decoding of Block Codes
6,301,681	2001	Messaging Communication Protocol
6,278,741	2001	Timing Recovery Circuit in QAM Modems
6,101,520	2000	Arithmetic Logic Unit and Method for Numerical Computations in Galois Fields
6,052,812	2000	Messaging Communication Protocol
5,898,737	1999	Adaptive Digital Symbol Recovery for Amplitude Phase Keyed Digital Communication Systems
5,972,799	1999	Global Parity Symbol for Interleaved Reed-Solomon Coded Data
5,812,438	1998	Arithmetic Logic Unit and Method For Numerical Computations in Galois Fields
5,787,099	1998	System And Method for Encoding And Decoding Data Using Numerical Computations in Galois Fields
5,751,769	1998	Programmable Digital Linear and Nonlinear Transversal Equalizer
5,771,184	1998	System and Method For Solving Quadratic Equation in Galois Fields
5,642,366	1997	Global Parity Symbol for Interleaved Reed-Solomon Coded Data
5,442,663	1995	Residual Carrier Adaptive Cross-Polarization Equalizer
4,958,349	1990	High Data Rate Bch Decoder

Publications:

R.M. Orndorff, T.W. Doak & R.W. Koralek, "CMOS/SOS LSI Implementation of Viterbi Error Correction Circuitry," IEEE International Solid State Circuits Conference (ISSCC), February 1979

R.A. Freund and R.W. Koralek, "A Technique for Testing LSI Closed Loop Networks," 1979 IEEE Test Conference, October 1979

R.M. Orndorff, J.D. Krzmarik, R.J. Colesworthy, T.W. Doak and R.W. Koralek, "Viterbi Decoder VLSI Integrated Circuit for Bit Error Correction," 1981 IEEE National Telecommunications Conference, November 1981

F. Chethik, F. J. Smith and R. W. Koralek, "System approaches and technologies for satellite data microwave transmission approaching 8 gigabits per second," 1994 IEEE National Telesystems Conference, May 1994